WHAT IS CLAIMED IS:

1. A method for fabricating a metallic bit-line contact on a semiconductor substrate having disposed thereon, at least, a trench capacitor, an associated select transistor and a diffusion region, which forms a source/drain electrode of the select transistor, the method comprising:

forming an insulator layer to the semiconductor substrate;

forming a bit-line contact hole in the insulator layer to expose at least a portion of the source/drain electrode;

doping at least the exposed portion of the source/drain electrode;

annealing at least the doped portion of the source/drain electrode;

depositing a liner layer on at least the exposed portion of the source/drain electrode; and

depositing at least one of a metal and a metal alloy in order to fill the bit-line contact hole.

2. The method as claimed in claim 1, wherein the liner layer is deposited using at least one of a sputtering process, a chemical vapor deposition process and an atomic layer deposition process.

3. The method as claimed in claim 1, wherein doping comprises ion implantation to form a locally delimited electrical contact layer with relatively reduced lateral migration underneath the insulator layer.

4. The method as claimed in claim 1, wherein the annealing is performed on any substrate damage caused during the doping.

5. The method as claimed in claim 1, wherein the at least one of the metal and the metal alloy comprises tungsten, aluminum or copper.

6. The method as claimed in claim 1, wherein the liner layer comprises at least one of Ti and Ti/TiN.

7. The method as claimed in claim 1, wherein forming the bit-line contact hole in the insulator layer comprises patterning the insulator layer;

8. The method as claimed in claim 7, wherein the patterning of the bit-line contact is carried out with the aid of the dual-damascene process.

9. The method as claimed in claim 1, further comprising:

forming a peripheral contact hole on the semiconductor substrate; and

filling the peripheral contact hole with the at least one of the metal and the metal alloy as part of the same process as depositing at least one of the metal and the metal alloy in order to fill the bit-line contact hole.

10. The method as claimed in claim 9, further comprising doping a surface exposed by the peripheral contact hole while doping at least the exposed portion of the source/drain electrode and wherein doping both the surface exposed by the peripheral contact hole and the exposed portion of the source/drain electrode using a same mask.

11. A memory cell formed on a substrate, comprising:

a trench capacitor; and

a select transistor, comprising:

a diffusion region forming a source/drain electrode of the select transistor;

a bit-line contact formed in an insulator layer and comprising a filling comprising at least one of a metal and a metal alloy, wherein the bit-line contact connects the source/drain region to an associated bit line; and

a doped region between the substrate and the filling of the bit-line contact.

12. The memory cell of claim 11, wherein the doped region is formed on the source/drain region.

13. The memory cell of claim 11, wherein the doped region comprises a locally limited electrically conductive contact layer, having a relatively reduced lateral migration underneath the insulator layer.

14. The memory cell of claim 11, wherein the select transistor is at least partially disposed in the substrate and the trench capacitor is completely disposed in the semiconductor substrate.

15. The memory cell of claim 11, wherein the bit-line contact comprises at least one of tungsten, aluminum and copper.

16. The memory cell of claim 11, wherein the memory cell is part of a memory cell arrangement comprising peripheral contacts are formed in a same structure plane and comprising a filling substantially similar to that of the bit-line contact.

17. The memory cell of claim 11, the bit-line contact further comprising a liner layer formed between the substrate and the filling of the bit-line contact.

18. The memory cell of claim 17, wherein the liner layer comprises at least one of Ti and Ti/TiN.

19. A memory cell formed on a substrate, comprising:

a trench capacitor; and

a select transistor, comprising:

a diffusion region forming a source/drain electrode of the select transistor;

a bit-line contact formed in an insulator layer and comprising a filling comprising at least one of a metal and a metal alloy, wherein the bit-line contact connects the source/drain region to an associated bit line;

a doped region formed on the source/drain region between the substrate and the filling of the bit-line contact; and

an annealed region formed as a result of an anneal process performed during fabrication of the bit-line contact.

20. The memory cell of claim 19, wherein the annealed region includes a damaged region damaged during a doping processed performed to form the doped region.

21. The memory cell of claim 19, wherein the annealed region includes at least a portion of the doped region.

22. The memory cell of claim 19, the bit-line contact further comprising a liner layer formed between the substrate and the filling of the bit-line contact.